REMARKS

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, Applicants have amended various of their claims to recite a circuit tape with an adhesive film, and have amended their claims throughout to refer to an adhesive film, rather than an adhesive layer. In addition, Applicants have further amended claims 1, 11 and 19 to recite that an elastic modulus of the adhesive film at room temperature is equal to or less than 4000 MPa. In light of the foregoing amendments, Applicants have canceled claims 3, 6 and 16 without prejudice or disclaimer.

In addition, Applicants are adding new claims 34 and 35 to the application. Claims 34 and 35, each dependent on claim 24, respectively recites the subject matter as expressly set forth in previously considered claims 6 or 16, and in claim 29, respectively.

The objection to the disclosure on the basis of informalities, as listed on page 2, lines 1-3 of the Office Action mailed May 12, 2005, is noted. Applicants have reviewed their Specification at the pages and lines listed by the Examiner (for example, page 9, line 16) and do not find the phrases objected to. It is respectfully requested that the Examiner contact the undersigned so as to discuss the objections to the disclosure; and, in particular, the specific portions of Applicants' Specification containing the expressions objected to by the Examiner.

The obviousness-type double patenting rejections as set forth on pages 10-13 of the Office Action mailed May 12, 2005, are noted. Also noted is the indication by the Examiner that a timely filed Terminal Disclaimer in compliance with 37 CFR §1.321(c) may be used to overcome a double patenting rejection.

In view of the foregoing, submitted herewith is an Terminal Disclaimer for the above-identified application, with respect to U.S. Patent No. 6,114,753. It is

respectfully submitted that the enclosed Terminal Disclaimer, together with the fee submitted therewith, satisfy requirements of 37 CFR §1.321(c). In view of the present submission of this Terminal Disclaimer, it is respectfully submitted that the obviousness-type double patenting rejections are moot.

The enclosed Terminal Disclaimer is being presently submitted in order to facilitate proceedings in connection with the above-identified application, so as to achieve earliest possible issuance of a U.S. patent based upon the above-identified application. It is respectfully submitted that the present filing of this Terminal Disclaimer does not constitute agreement with, or an admission as to the propriety of, the obviousness-type double patenting rejections; and does not constitute agreement with, or an admission as to the propriety of, arguments made by the Examiner in connection with this obviousness-type double patenting rejections.

Applicants respectfully submit that all of the claims presented for consideration by the Examiner patentably distinguish over the teachings of the references applied by the Examiner in rejecting claims in the Office Action mailed May 12, 2005, that is, the teachings of the U.S. patents to Freyman, et al., No. 5,646,451, and to Lee, et al., No. 5,620,928, Japanese Patent Document No. 06-236906 (Akikuni), and the article by Nakayoshi, et al., "Memory Package With LOC Structure Using New Adhesive Material," in IEEE 1994, pages 575-579, under the provisions of 35 USC §102 and 35 USC §103.

It is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a circuit tape with an adhesive film, or such adhesive film, as in the present claims, adapted to be used in ball grid array semiconductor devices, and wherein an elastic modulus of the adhesive film, in a range of mounting reflow temperature for mounting the semiconductor element onto a mounting substrate, is more than 1 MPa, and an

elastic modulus of the adhesive film at room temperature is equal to or less than 4000 MPa. See claims 1, 11 and 19.

Moreover, it is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such circuit tape with an adhesive film, adapted to be used in ball grid array semiconductor devices, having features as discussed previously, and additionally wherein each adhesive film has a size less than that of the elongated circuit tape to which the adhesive film is continuously adhered. See claim 11.

In addition, it is respectfully submitted that the teachings of the applied references would have neither disclosed nor would have suggested the other features of the present invention as in the present claims, having the features as discussed previously in connection with independent claims 1, 11 and 19, as appropriate, and, additionally, wherein the adhesive film has an elastic modulus, in the range of 200° – 250°C, of more than one MPa (see claims 2 and 13); and/or wherein the adhesive film has a layer of thermoplastic resin which has a glass transition temperature greater than 250°C (see, e.g., claim 8); and/or the coefficient of moisture absorption of material of the adhesive film, as in, e.g., claim 9; and/or wherein the circuit tape has an uneven surface with spaces between portions of the circuit, the adhesive film filling in the spaces (see claim 10); and/or wherein the circuit tape includes pads for electrical connection thereto by a ball grid array connection (see claims 28 and 32).

The present invention relates to an adhesive film, and to a circuit tape including such adhesive film, particularly appropriate in connection with mounting semiconductor devices having a high density on the circuit tape.

In the continuing effort to improve electronic devices in order to provide high performance, demand for high integration of semiconductor devices and high density

mounting of semiconductor elements of such devices has become more important. As one technique for responding to increased number of pins of semiconductor elements, a grid array structure has come to be used in mounting. Such grid array structure includes a ball grid array structure, which has a shortened connecting terminal length in order to enable fast signal transmission. Moreover, in order to provide increased speed of signal transmission, organic materials having a relatively low dielectric constant have been investigated for use in multilayer carrier substrates. However, the organic materials generally have a larger thermal expansion coefficient than that of the semiconductor element, and, therefore, thermal stress is generated by the difference in thermal expansion, and becomes a problem from the point of view of, for example, connection reliability.

It has been proposed to use an elastomer material having a low modulus of elasticity for reducing the thermal stress generated by the difference in thermal expansion between the semiconductor element and the mounting substrate. A silicone material has generally been used as the elastomer material, the silicone having a low modulus elasticity and a superior heat resistance. However, such proposed technique has problems, such as a difficulty in maintaining the flatness of the silicone layer (which constitutes a stress buffer layer), and complexity of the printing process used for forming the adhesive layer.

Against this background, Applicants provide a circuit tape, and adhesive film, avoiding problems in connection with proposed prior techniques, and which provides a stress buffer layer superior in flatness and which avoids other problems such as voids being formed in the layer under high temperature conditions utilized, for example, in connecting the semiconductor element to the circuit tape. Applicants have found that by utilizing an adhesive film having an elastic modulus, in a range of mounting reflow temperature for mounting a semiconductor element onto a mounting

substrate, of more than one MPa, with this adhesive film having an elastic modulus at room temperature that is equal to or less than 4000 MPa, objectives of the present invention are achieved; and, in particular, the film has superior flatness while escaping faults such as voids being formed in the film during processing. Thus, the connection of the element to the substrate, utilizing the adhesive film of the present invention, is reliable. Note, for example, page 15, lines 7-16 of Applicants' Specification. Note also the paragraph bridging pages 18 and 19; the last full paragraph of page 36; and the paragraph bridging pages 36 and 37, of Applicants' Specification.

The article by Nakayoshi, et al. discloses a new adhesive tape for lead-on-chip structure, which is a single-layer thermoplastic polyimide siloxane. This article discloses that by providing a large Young's modulus of the film at high temperature and contamination-free lead surface, a sufficient lead-wire bondability can be achieved. Note also the Conclusion on page 579 of this article. See also Fig. 7 on page 578, and the description in connection therewith that the authors found that the adhesive which keeps high the Young's modulus during the wire bond process (that is, has high glass transition temperature) does not cause the deformation of inner leads and effectively conveys power to inner leads and gives high bondability.

It is respectfully that this reference does not disclose, nor would have suggested, an adhesive film having the elastic modulus both at the range of mounting reflow temperature for mounting the semiconductor onto a mounting substrate and at room temperature, as in the present claims, and advantages achieved thereby. In this regard, it is emphasized that Nakayoshi, et al. discloses on page 578 that the adhesive has the recited Young's modulus, and it is respectfully submitted that this reference would have neither disclosed nor would have suggested such feature of the present invention that the adhesive film, according to

the present invention, has the recited elastic modulus both in the range of mounting reflow temperature and at room temperature.

Even noting the teachings of Freyman, et al., it is respectfully submitted that the teachings of Nakayoshi, et al. in light of the teachings of Freyman, et al. do not teach, nor would have suggested, the presently claimed invention, including wherein the adhesive film has the recited elastic modulus at both room temperature and in a range of mounting reflow temperature, as in the present claims.

Freyman, et al. is directed to multifunctional chips, and in particular wherein the chip includes first and second electrically isolated bonding pads and also includes a control circuit coupled to the second bonding pad. This patent discloses, in a description of the background of the invention, that typical wire bonds are gold or aluminum and that a typical wire bonding temperature is 225°C.

Even in light of the teachings of Freyman, et al., it is respectfully submitted that the teachings of Nakayoshi, et al. would have neither taught nor would have suggested the presently claimed invention, including the adhesive film, wherein such film has elastic modulus both in the range of mounting reflow temperature and at room temperature, as in the present claims.

The contention by the Examiner that the recitation "adapted to be used in ball grid array semiconductor devices, which is for adhering a semiconductor element to circuit tape" has not been given "patentable weight" because the recitation occurs in the preamble, is respectfully traversed. Contrary to the contention by the Examiner, it is respectfully submitted that the "adapted to be used" recitation constitutes a property of the adhesive film, which must be given weight in determining patentability. While the Examiner has indicated that the "adapted to be used" language has not been given "patentable weight," such statement is not understood. If the Examiner has given this recitation no weight (that is, has ignored this

recitation), then it is respectfully submitted that the Examiner is clearly erroneous in interpretation of the claims.

In any event, it is emphasized that Nakayoshi, et al. discloses an adhesive tape for lead-on-chip structure, and the Examiner has not even alleged that such tape is "adapted to be used" in ball grid array semiconductor devices, for connecting a semiconductor element to the circuit tape.

Akikuni discloses an adhesive tape for a semiconductor, wherein an adhesive layer and a protective layer are provided on an insulating film, and wherein the Young's modulus after hardening of the adhesive layer, is 4×10^8 dyne/cm^2 or greater.

It is respectfully noted that Akikuni discloses a Young's modulus of the adhesive layer, which forms only a part of the adhesive tape. It is respectfully submitted that Akikuni would have neither disclosed nor would have suggested the adhesive film as in the present claims, wherein the adhesive film (for example, not just the adhesive layer thereof) has the elastic modulus both in a range of mounting reflow temperature for mounting the semiconductor element onto a mounting substrate, and at room temperature.

The contention by the Examiner that Akikuni discloses an elastic modulus of the adhesive film, in a range of mounting reflow temperature for mounting a semiconductor element onto a mounting substrate, of more than one MPa, is respectfully traversed. It is emphasized that Akikuni discloses the Young's modulus of the adhesive layer; and it is respectfully submitted that the disclosure of this patent document would have neither taught nor would have suggest the Young's modulus of the adhesive tape disclosed therein, as in the present claims.

It is respectfully submitted that the combined teachings of Lee, et al. and of Nakayoshi, et al. would have neither taught nor would have suggested the presently claimed subject matter.

Lee, et al. discloses ultra thin ball grid array integrated circuit packages, using a temporary supporting substrate carrier to support the components of the package during the assembly of the package. This patent discloses that the integrated circuit package assembly includes a dielectric flex tape substrate, an integrated circuit die, and an encapsulating material. The dielectric flex tape substrate has a horizontal top surface, a horizontal bottom surface, an outermost peripheral edge and a plurality of electrically conductive traces and/or contacts accessible from outside the assembly. The bottom surface of the integrated circuit die is attached to the top surface of the flex tape substrate. Note the paragraph bridging columns 2 and 3 of this patent. See also column 2, lines 7-37, for a technique of manufacturing the integrated circuit package assembly. See also column 3, lines 57-65. This patent goes on to disclose that the die and substrate 42 (See Fig. 2A) are attached to substrate carrier 38 using a double-side adhesive tape material 70, one example of such adhesive material being double-sided polyimide tape. See column 4, lines 25-36. Note also the paragraph bridging columns 5 and 6 of Lee, et al., describing three additional embodiments and wherein the die 40 is attached to substrate 84 using, for example, conventional die attached material 87 (Note Figs. 4A-C).

Nakayoshi, et al., and Freyman, et al. have been previously discussed.

Initially, it is respectfully submitted that the teachings of Nakayoshi would not have been properly combinable with the teachings of Lee, et al. That is, Lee, et al. is directed to the technology of ball grid arrays, while Nakayoshi, et al. is directed to lead-on-chip technology. It is respectfully submitted that one of ordinary skill in the art concerned within Lee, et al. would not have looked to the lead-on-chip technology

as in Nakayoshi, et al. In connection therewith, the contention by the Examiner that Lee, et al. and Nakayoshi, et al. are analogous art, the Examiner pointing to the specification of the above-identified application as disclosing use of an LOC film as an adhesive for a circuit tape for a ball grid array semiconductor device, is noted. It is respectfully submitted that the Examiner is improperly using the teachings of Applicants' specification against Applicants, which is clearly erroneous under the requirements of 35 USC §103. It is respectfully submitted that the Examiner has provided no proper basis for concluding that LOC and ball grid array arts are analogous.

The additional contention by the Examiner that the applied references are analogous art "because they are directed to a similar problem-solving area of semiconductor device packaging" is respectfully traversed. Thus, note that Nakayoshi, et al., is directed to LOC structure to secure sufficient lead-wire bondability. In contrast, the ball grid array structure, in, for example, Lee, et al. would not have lead-wire bonding. Clearly, Lee, et al. and Nakayoshi, et al. do not address similar problem-solving areas.

In addition, it is respectfully submitted that the Examiner has not provided proper motivation in connection with combining the teachings of Lee, et al. and Nakayoshi, et al., especially in view of the differing technologies and differing problems addressed by each.

In any event, even assuming, arguendo, that the teachings of Lee, et al. and Nakayoshi, et al. were properly combinable, and even in light of the teachings of Freyman, et al., it is respectfully submitted that the combined teachings of these references would have neither disclosed nor would have suggested the presently claimed subject matter, including, inter alia, the elastic modulus of the adhesive film, both in a range of mounting reflow temperature for mounting the semiconductor

element onto a mounting substrate, and at room temperature, and advantages thereof.

It is respectfully submitted that the combined teachings of Lee, et al. and of Akikuni would have neither disclosed nor would have suggested the presently claimed subject matter.

Both Lee, et al. and Akikuni have been previously discussed. Noting, in particular, the previous discussion that Akikuni discloses a Young's modulus after hardening of the adhesive layer, which forms part of the adhesive tape together with the insulating film 1 and protective layer 3, it is respectfully submitted that the combined teachings of Lee, et al. and of Akikuni would have neither disclosed nor would have suggested such circuit tape or such adhesive film as in the present claims, wherein the adhesive film has the elastic modulus both in a range of mounting reflow temperature for mounting the semiconductor element onto the mounting substrate and at room temperature as in the present claims, and advantages thereof; and/or the other features of the present invention as discussed in the foregoing, and advantages thereof.

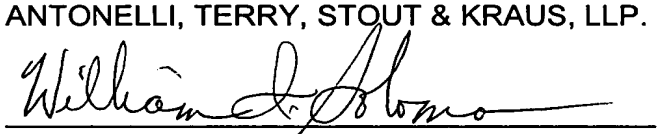
The Examiner is thanked for the indication of allowable subject matter, set forth on page 13 of the Office Action mailed May 12, 2005. In view of the foregoing, it is respectfully submitted that all claims being considered on the merits in the above-identified application, including the independent claims, should be allowed; and, accordingly, it is respectfully submitted that Applicants need not set forth the claims listed in the next-to-last paragraph on page 13 of the Office Action mailed May 12, 2005, in independent form, in order for these claims to be allowed.

In view of the foregoing comments and amendments, reconsideration and allowance of all claims remaining in the above-identified application and being considered on the merits therein, are respectfully requested.

If the Examiner believes that there are any matters which can be resolved by way of either a personal or telephone interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

Applicants request any shortage or excess in fees in connection with the filing of this paper, including extension of time fees, and for which no other form of payment is offered, be charged or credited to Deposit Account No. 01-2135 (Case: 503.35443CC4).

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP.



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